**IN THE UNITED STATES DISTRICT COURT**
**FOR THE EASTERN DISTRICT OF TEXAS**
**MARSHALL DIVISION**

| | | |
|---|---|---|
| INVENSAS CORPORATION, | § | |
| | § | |
| Plaintiff, | § | |
| | § | |
| v. | § | |
| | § | No. 2:17-CV-00670-RWS-RSP |
| SAMSUNG ELECTRONICS CO., LTD., | § | |
| and SAMSUNG ELECTRONICS | § | |
| AMERICA, INC., | § | |
| | § | |
| Defendants. | § | |

## CLAIM CONSTRUCTION OPINION AND ORDER

This lawsuit concerns U.S. Patents 6,054,336, 6,232,231, 6,566,167, 6,825,554, and 6,849,946, which relate to various methods of manufacturing semiconductor devices. The ’231 and ’946 Patents concern methods of providing a substantially planar semiconductor topography, which facilitates the formation of high-resolution features in such devices. ’231 Patent at 1:28–48 (discussing problems associated with insufficiently planar topography during the manufacturing process); ’946 Patent at 1:32–52 (same). The ’167 and ’554 Patents teach using a ground trace in a particular configuration to provide noise shielding from other signals within the device. ’167 Patent at (57); ’554 Patent at (57). The ’336 Patent concerns methods of making conductor tracks on the semiconductor device in a way that provides very narrow gaps between the tracks while minimizing the possibility of short circuits between them due to their close proximity. ’336 Patent at 1:59–67. The ’336 Patent

thus facilitates a size reduction relative to prior art semiconductor devices because the spacing between tracks is reduced.

Having considered the parties' briefing and arguments of counsel during an August 22, 2018 claim construction hearing, the Court construes the disputed claim terms as follows.

## I. GENERAL LEGAL STANDARDS

### A. Claim Construction

"[T]he claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc). As such, if the parties dispute the scope of the claims, the court must determine their meaning. *See, e.g., Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 390 (1996), *aff'g*, 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc); *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1317 (Fed. Cir. 2007).

When construing claims, "[t]here is a heavy presumption that claim terms are to be given their ordinary and customary meaning." *Aventis Pharm. Inc. v. Amino Chems. Ltd.*, 715 F.3d 1363, 1373 (Fed. Cir. 2013) (citing *Phillips*, 415 F.3d at 1312–13). Courts must therefore "look to the words of the claims themselves . . . to define the scope of the patented invention." *Id.* (citations omitted). The "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1313. This "person of ordinary skill in the art is deemed to read the

claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.*

Intrinsic evidence is the primary resource for claim construction. *See Power-One, Inc. v. Artesyn Techs., Inc.*, 599 F.3d 1343, 1348 (Fed. Cir. 2010) (citing *Phillips*, 415 F.3d at 1312). For certain claim terms, "the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words." *Phillips*, 415 F.3d at 1314. But for claim terms with less-apparent meanings, courts consider "those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean . . . [including] the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art." *Id.*

## II. CONSTRUCTION OF DISPUTED TERMS[1]

### A. "substantially planar" / "substantially coplanar" ('231 Patent, cl.1, 4; '946 Patent, cl.16, 17)

| Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|
| Plain and ordinary meaning, no construction necessary. Alternatively, "substantially flat or level" and "substantially at the same elevation," respectively | Indefinite |

The '231 and '946 Patents, which share the same specification,[2] teach preventing the formation of elevational disparities during the semiconductor manufacturing process. Any such disparities can negatively affect subsequent steps in the manufacturing process and cause incorrect patterning of layers when using lithography. '231 Patent at 1:27–41.

Elevational disparities can form when a conductive material is deposited across an uneven surface. The conductive material fills laterally separated trenches formed in the substrate. The trenches provide well-known technical benefits not important to the asserted patents. Ideally, the conductive material above the top surface of the substrate could be removed using chemical-mechanical polishing (CMP), a process using a polishing pad and

[1] At the time of the Court's claim construction hearing, the parties had not agreed to constructions for any claim terms. *See* P.R. 4-5 Joint Notice Regarding Cl. Constr. Chart [Dkt. # 142] at 1 ("The parties have not agreed to any constructions at this time.").

[2] The application that became the '946 Patent is a continuation of the application that became the '231 Patent. '231 Patent at (65); *id.* at 1:6–8. Accordingly, the '231 and '946 Patents share the same specification.

an abrasive slurry. *Id.* at 1:52–63. In sections with a wide trench, however, the polishing pad tends to conform to the surface topography, causing the surface material of recessed areas to be stripped. *Id.* at 3:14–22, FIG. 4 (showing a recessed area (42) attributable to the polishing pad conforming to the surface topography). In sections with many narrower trenches, the slurry may react with the conductive metal at a different rate than with the surrounding oxide. This causes the metal to be removed at a faster rate than the surrounding oxide, also resulting in a recessed area. *Id.* at 3:23–42, FIG. 4 (showing a recessed area (40) attributable to oxide erosion)

To address the problem, the ’231 and ’946 Patents generally teach forming “dummy” trenches in the dielectric layer so the conductive material is deposited into the additional trenches. This causes the conductor material and dielectric to react to the slurry at approximately the same rate over the entire area. *See id.* at 4:30–32 (“Advantageously, the polish rate of the conductive material above the dummy trenches and the wide and narrow trenches is substantially uniform.”). The conductor material within a dummy trench is not connected to an integrated circuit or other electrical components. *Compare* Pl.’s Br. [Dkt. # 123] at 13, *with* Defs.’ Br. [Dkt. # 134] at 6 (both proposing a construction whereby the dummy conductors “are not connected to any active or passive devices that function as an integrated circuit”).

The parties’ dispute concerning “substantially planar” and “substantially coplanar” relates to indefiniteness. Defendants contend “the intrinsic record provides no objective

standard or boundary to define the degree of flatness that qualifies as 'substantially planar/co-planar.'" Defs.' Br. [Dkt. # 134] at 1. Thus, say Defendants, these terms are indefinite. *Id.* Plaintiff counters that a person of ordinary skill would understand that no semiconductor layer is perfectly flat and that the degree of planarity will vary depending on tolerances of the particular fabrication process. Pl.'s Br. [Dkt. # 123] at 10.

"[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2124 (2014). The claims "must be precise enough to afford clear notice of what is claimed," but that consideration must be made while accounting for the inherent limitations of language. *Id.* "As long as claim terms satisfy this test, relative terms and words of degree do not render patent claims invalid." *One-E-Way, Inc. v. I.T.C.*, 859 F.3d 1059, 1063 (Fed. Cir. 2017); *see also Tinnus Enter., LLC v. Telebrands Corp.*, 733 Fed. App'x 1011, 1018 (Fed. Cir. 2018) (finding that using "substantially" did not render the term indefinite).

Here, "substantially planar" and "substantially coplanar" do not render the claims indefinite to a person of ordinary skill.[3] The patents describe the known problem of eleva-

[3] Although Plaintiff proffers a level of ordinary skill in the art, Pl.'s Br. [Dkt. # 123] at 2–3, Defendants do not. Accordingly, the Court concludes Defendants agree with Plaintiff's proffered level of ordinary skill for purposes of claim construction.

tional disparities and the increasing use of CMP to planarize and remove surface irregularities. Clearly, perfect planarization would be the goal, even though it might be unattainable at an atomic level. Nevertheless, the Court finds a person of ordinary skill would understand the meaning of "substantially planar" and "substantially coplanar" as these terms relate to avoiding the formation of elevational disparities during the manufacturing process. For the disputed phrases "substantially planar" and "substantially coplanar," the Court adopts the Plaintiff's proposed construction of plain and ordinary meaning.

### B. "trench" ('231 Patent, cl.1, 3, 4; '946 Patent, cl.16–17, 20–22)

| Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|
| a cavity, or recess, formed in a semiconductor substrate or a dielectric layer | plain and ordinary meaning; no construction necessary |

Plaintiff argues "trench" is a term of art and that, in semiconductor manufacturing, a "trench" can be any size or shape. Pl.'s Br. [Dkt. # 123] at 11–12. Defendants counter that "trench" is a lay term that has a well-understood meaning that the jury can apply without a construction. Defs.' Br. [Dkt. # 134] at 5.

The Court preliminarily construed "trench" as having its plain and ordinary meaning, but rejected any requirement of a particular shape. During the hearing, Defendants agreed that "trench" has no dimensional restrictions. H'rg Tr. [Dkt. # 178] at 36:24–25. And all parties agreed with the Court's preliminary construction, as well as the lack of a restriction on the depth of a "trench." *Id.* at 37:3–4; *see also id.* at 40:1–7.

Based on the parties' agreement at the hearing, "trench" should be given its plain and ordinary meaning. The term does not require any particular shape (e.g., that a "trench" must be elongated) or depth.

### C. "dummy conductors" ('231 Patent, cl.1, 12; '946 Patent, cl.16–18)

| Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|
| Plain and ordinary meaning, no construction necessary. Alternatively, "conductive structures that are not connected to any active or passive devices that function as an integrated circuit." | conductive structures that can carry power or ground voltages but are not connected to any active or passive devices that function as an integrated circuit |

The parties propose similar constructions for "dummy conductors," but dispute whether the proper construction of "dummy conductors" requires the capability to carry power and ground voltages. Defendants contend the specification defines "dummy conductors" as requiring that capability. Defs.' Br. [Dkt. # 134] at 6 (citing '231 Patent at 8:4–9; *id.* at 4:35–44). Plaintiff argues Defendants' construction excludes embodiments from the patents, because none of the figures depict any connection from the dummy conductors to a power supply or ground. Pl.'s Br. [Dkt. # 123] at 15.

The Court agrees with Plaintiff. The claims recite structure, yet the proposed phrase "can carry power or ground voltages" recites a capability. The phrase is also redundant of "conductive," which the parties agree is part of the proper construction. Moreover, the language from the specification on which Defendants rely does not define the term expressly or by implication. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir.

1996) ("The specification acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication."). To the contrary, the specification implies that dummy conductors might *not* be connected to a power supply or ground. *See id.* at 4:35–44 ("*Most likely*, the dummy conductor are connected to a power supply or ground . . ." (emphasis added)). For these reasons, the Court construes "dummy conductors" to mean "conductive structures that are not connected to any active or passive devices that function as an integrated circuit."

### D. "conductive lines" ('946 Patent, cl.16, 19)

| Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|
| Plain and ordinary meaning, no construction. Alternatively, "a line of conductive material." | conductive structures that are connected to one or more active or passive devices that function as an integrated circuit |

This disputed term appears in two claims of the '946 Patent. Claim 16 requires

> a plurality of laterally spaced dummy trenches in a dielectric layer, between a first trench and a series of second trenches . . . ;
>
> dummy conductors in said laterally spaced dummy trenches . . . ; and
>
> conductive lines in said series of second trenches and said first trench . . . .

'946 Patent at 10:25–42. Claim 19 simply limits the "conductive lines" to specific metals. *Id.* at 54–58.

Defendants argue that "conductive lines" as used in Claim 16 must be connected to

active or passive integrated circuits. Defs.' Br. [Dkt. # 134] at 8. They note the specification never uses the term "conductive lines" and infer that the term equates to "interconnects." *Id.* Defendants also argue that because the dummy connectors are not connected to integrated circuits, the conductive lines must be so connected. *Id.* at 7–8. Plaintiff, however, stresses that "conductive lines" and "interconnect" are used differently in the claims. Pl.'s Reply [Dkt. # 141] at 3–4.

The Court agrees with Plaintiff for two reasons. First, the patentee did not define "conductive lines" to have the same meaning as "interconnect," which suggests a structure that connects two things together.[4] Rather, other claims of the '946 Patent use "interconnect," and the Court presumes that different claim terms have different meanings. *Nystrom v. TREX Co.*, 424 F.3d 1136, 1143 (Fed. Cir. 2005) ("When different words or phrases are used in separate claims, a difference in meaning is presumed." (citing *Tandon Corp. v. I.T.C.*, 831 F.2d 1017, 1023 (Fed. Cir. 1987)). Defendants have not overcome that presumption, and the Court rejects the argument that "conductive lines" must be connected to devices because the "dummy conductors" are not so connected.

Second, although both the "conductive lines" and "dummy conductors" could be made from the same physical material (e.g., copper), the structural distinction between

[4] *See* http://www.yourdictionary.com/interconnect#websters?direct_search_result=yes (defining "interconnect" as "[t]o be connected with each other," or "to connect reciprocally").

them is their location within the claimed invention. The claims require "a plurality of laterally spaced dummy trenches . . . between a first trench and a series of second trenches." '946 Patent at 10:27–29. The claims further require that (1) the dummy conductors are in the dummy trenches, and (2) the conductive lines are in the first trench and the series of second trenches. *Id.* at 10:36–42. These requirements do *not* speak to whether these elements are connected to other devices, and the Court sees no basis for reading such a requirement into the claims. Accordingly, "conductive lines" does not require connection to devices that function as an integrated circuit. For the disputed phrase "conductive lines," the Court adopts the Plaintiff's proposed construction of plain and ordinary meaning.

### E. "plurality of laterally spaced dummy trenches" ('231 Patent, cl.1; '946 Patent, cl.16)

| Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|
| Plain and ordinary meaning, no construction. Alternatively, "two or more dummy trenches arranged with spaces between their sides." | two or more separate dummy trenches arranged with spaces between their sides |

The parties dispute how to determine whether there are multiple trenches in an accused device. Defendants contend that separate dummy trenches must be completely isolated from one another. Defs.' Br. [Dkt. # 134] at 10–11. Plaintiff argues that such a requirement would be inconsistent with the claim language. *Id.* at 17.

The intrinsic record does not suggest multiple trenches cannot connect or intersect. Indeed, even the addition of "separate" to the construction, as Defendants urge, does not

resolve that dispute, as "separate trenches" might still be connected. Accordingly, "plurality of laterally spaced dummy trenches" should be given its plain and ordinary meaning, and there is no requirement that the "dummy trenches" cannot connect or intersect.

### F. "forming a conductor pattern on the conductive layer" ('336 Patent, cl.1)

| Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|
| forming a pattern to be transferred to the conductive layer | forming a pattern in the conductive layer with gaps corresponding to the auxiliary windows |

The '336 Patent claims methods of forming conductor tracks on an electronic device. Claim 1, for example, recites:

> providing an electrically insulating substrate;
>
> providing a conductive layer on the substrate;
>
> forming a conductor pattern on the conductive layer by forming windows at the conductor layer, the step of forming the windows at the conductor layer comprising:
>
> providing a first dielectric layer adjacent the substrate and having a thickness;
>
> forming auxiliary windows in the first dielectric layer having dimensions which are greater, in at least one dimension, than the windows to be formed at the conductor layer, the auxiliary windows having sidewalls which define a depth of the auxiliary windows which depth is only part of the thickness of the first dielectric layer;
>
> providing an additional dielectric layer on the first dielectric layer including over the auxiliary windows formed in the first dielectric layer;

> etching the additional dielectric layer back anisotropically without a mask to form spacers on the sidewalls of the auxiliary windows, which spacers are formed by unetched portions of the additional dielectric layer; and
>
> continuing etching anisotropically through the auxiliary window and the spacers to define the windows at the conductive layer.

'336 Patent at 5:17–42. Claim 5, which indirect depends from Claim 1, recites that "the conductor pattern is formed *in* the conductive layer" by oxidizing the portions of the conductive layers exposed through the auxiliary windows. *Id.* at 6:16–20 (emphasis added).

The parties dispute the meaning of "forming a conductor pattern *on* the conductive layer" in Claim 1. Defendants contend this step requires forming the pattern *in* the conductive layer because this is how the patent achieves its object of ensuring gaps smaller than the "auxiliary windows" formed using lithography. Defs.' Br. [Dkt. # 134] at 16–17. Plaintiff contends the claims distinguish between forming a pattern "on" the conductive layer and "in" the conductive layer. Pl.'s Br. [Dkt. # 123] at 18 ("While claim 1 refers to the conductor pattern 'on' the conductive layer, claim 5 refers to the conductor pattern 'formed *in* the conductive layer.'" (emphasis added)). Plaintiff also contends the claims are consistent with creating a mask that can then be used to form gaps in the conductive layer. *Id.* at 19. Defendants attack Plaintiff's construction as leaving the forming of the pattern ambiguous so that it could include gaps outside of the axillary windows. Defs.' Br. [Dkt. # 134] at 17.

Plaintiff's construction is better supported by the claim language and intrinsic record. The phrase requires "forming windows *at* the conductive layer." '336 Patent at 5:21–22 (emphasis added). Although "at" can mean "in," it can also mean "on" or "near."[5] Consistent with the latter meanings, the steps of "providing a first dielectric layer," "providing an additional dielectric layer," "etching the additional dielectric layer," and "continuing etching anisotropically" correspond to the specification's description of FIGS. 1(a)–1(g). FIG. 1(h), on the other hand, shows the embodiment after removal of the silicon oxide layer, which corresponds to dependent Claim 5. '336 Patent at 6:16–20 (reciting "the conductor pattern [being] formed *in* the conductive layer" (emphasis added)). Also, the '336 Patent's use of "in" in Claim 5 suggests the most logical reading of the disputed language, read in light of the specification and particularly FIG. 1, is that Claim 1 is directed to all of the steps *except* the oxidation of the conductor layer. For these reasons, the Court construes the disputed phrase "forming a conductor pattern on the conductive layer" to mean "forming a pattern to be transferred to the conductive layer."

### G. "continuing etching anisotropically through the auxiliary window and the spacers to define the windows at the conductive layer" ('336 Patent, cl.1)

| Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|
| Plain and ordinary meaning, no construction. | without interruption, to go on etching anisotropically only the portions of the first dielectric layer within the auxiliary window |

[5] http://www.yourdictionary.com/at?direct_search_result=yes

The parties dispute two aspects of this phrase. First, the parties dispute the locations of the windows defined at the conductive layer. Second, the parties dispute whether there can be an interruption in time between the "etching" step and the "continuing etching" step.

As to the first issue, Defendants contend the specification's emphasis on forming gaps narrower than what prior art lithography could achieve mandates limiting the etching to only the portions of the conductive layer within the auxiliary window. Defs.' Br. [Dkt. # 134] at 18–21. Plaintiff, however, contends such a construction would read out every disclosed embodiment. Pl.'s Br. [Dkt. # 123] at 22.

"[W]here the specification makes clear at various points that the claimed invention is narrower than the claim language might imply, it is entirely permissible and proper to limit the claims." *Alloc, Inc. v. I.T.C.*, 342 F.3d 1361, 1370 (Fed. Cir. 2003) (quoting *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1345 (Fed. Cir. 2001). Here, however, Defendants seek not to limit the steps of the method claim, but to limit the *result* of implementing the recited steps. The '336 Patent describes the objective of forming windows "in the dielectric layer . . . which are substantially smaller than the dimensions of the original windows." '336 Patent at (57). That objective is accomplished using the steps of Claim 1, which already limits the size of the auxiliary windows relative to the windows to be formed in the dielectric layer. *Id.* at 5:25–28 (reciting "forming auxiliary windows in the first dielectric layer having dimensions which are greater, in at least one dimension, than the windows to be formed at the conductor layer"). That size limitation is consistent

with the scope of invention set forth in the abstract. *See also id.* at (57). There is no basis for further limiting the scope of the disputed phrase.

As for the second issue—whether Claim 1 requires a stoppage between the two "etching" steps—Defendants contend that the specification does not disclose two separate and distinct etching processes with an interruption between them. Defs.' Br. [Dkt. # 134] at 21–22. But that alone is not enough to warrant limiting the term for two reasons. First, the specification is silent about whether there is any temporal spacing between the "etching" and "continuing etching" steps. Second, the claims strongly suggest that the demarcation between the two steps is not time, but rather the formation of spacers on the sidewalls of the auxiliary windows. Accordingly, the Court rejects this aspect of Defendants' proposed construction and adopts Plaintiff's proposed construction of plain and ordinary meaning.

### H. "providing a first dielectric layer adjacent the substrate" ('336 Patent, cl.1)

| Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|
| providing a first dielectric layer near the substrate | Plain and ordinary meaning, no construction necessary. |

Plaintiff believes Defendants want to argue that "adjacent" requires the first dielectric layer to be provided directly on the substrate. Defendants respond they have no intention of arguing non-infringement based on their original proposal for "adjacent," which was "without intervening layers." At the hearing, Defendants agreed that "adjacent" does

not mean "without intervening layers." H'rg Tr. [Dkt. # 178] at 114:17–19. Based on that agreement, this term should be given its plain and ordinary meaning.

### I. "row of solder balls" ('167 Patent, cl.1, 6, 11, 12; '554 Patent, cl.1)

| Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|
| three or more solder balls arranged next to each other in a line | three or more solder balls arranged next to each other in a horizontal or vertical line |

The '167 and '554 Patents[6] relate to methods of fabricating semiconductors using an array of solder balls to reduce electrical noise between adjacent signals in the device. The patents describe the then-conventional use of enhanced plastic ball grid arrays (EP-BGAs), which are wire bond packages that use 4-layer organic substrate for better electrical and thermal performance. '167 Patent at 1:37–41. Four-layer EPBGAs cost 20%–30% more than 2-layer PBGAs, prompting the need for fabricating a semiconductor package to reduce electrical noise in a 2-layer PBGA without adding the expensive additional layers. *Id.* at 1:53–56.

To address that need, the '167 and '554 Patents teach patterning a ground isolation trace to isolate signal traces, which provides noise shielding. *Id.* at 1:60–2:10. One embodiment of the invention uses a row of connected solder balls. More specifically, Claim 1 of the '167 Patent recites

[6] The application that became the '554 Patent is a division of the application that became the '167 Patent. '554 Patent at (62); *id.* at 1:4–5. Accordingly, the '554 and '167 Patents share the same specification.

(a) providing a 2-layer semiconductor substrate, the 2-layer substrate including a top layer and a bottom layer wherein the bottom layer includes an array of solder balls;

(b) patterning signal traces on the top layer;

(c) identifying groups of signal traces to isolate;

(d) patterning a grounded isolation trace adjacent to one of the groups of traces to isolate the signal traces and thereby provide noise shielding;

(e) identifying a row of solder balls to be grounded, and

(f) connecting the row of solder balls together and to ground to create a bottom-layer isolating ground trace.

*Id.* at 3:53–64. Similarly, Claim 1 of the ’554 Patent recites

a plurality of signal traces on a first layer;

at least one isolating ground trace on the first layer between two signal traces to provide noise shielding; and

an array of solder balls on a second layer such that at least one row of solder balls is connected together and to [g]round to create a second-layer isolating ground trace.

’554 Patent at 4:17–36.

The parties agree that “row of solder balls” should be construed as “three or more solder balls arranged next to each other in a line.” Defendants, however, argue the construction should reference “a horizontal or vertical” line. Defendants contend this additional language is supported by FIG. 4 of the patents, by the prior art referenced during prosecution, and by the use of “row” in the art. Defs.’ Br. [Dkt. # 134] at 28–29. Plaintiff notes the specification provides no mention of a specific horizontal or vertical orientation,

or any reason why a diagonal row should be excluded. Pl.'s Br. [Dkt. # 123] at 25. Plaintiff also contends the extrinsic evidence describes diagonal rows in the same way it describes horizontal or vertical rows. *Id.*

Common meanings of "row" support both constructions. According to one online dictionary, row could mean "a number of people or things arranged so as to form a line, esp[ecially] a straight line,"[7] which would support Plaintiff's broader construction. But the same dictionary has an alternative definition as "any of a series of such horizontal lines in parallel,"[8] which somewhat supports Defendants' narrower construction.

The Court adopts its preliminary construction, which is Plaintiff's proposed construction of "three or more solder balls arranged next to each other in a line." By limiting the row to a particular orientation, infringement potentially turns on the orientation of the accused device. For example, a horizontal row of solder balls in a first orientation may become a diagonal or vertical row of solder balls by simply rotating the arrangement 45 degrees or 90 degrees, respectively. The specification, however, does not suggest such an orientation-dependent construction. Nor does the specification disclose a technical reason for why the orientation of the linear arrangement of solder balls matters. At most, the specification describes the isolating ground trace as substantially parallel to one of the groups of signals to be isolated. *Id.* at 2:54–57. That, however, does not warrant the narrower construction advanced by Defendants.

[7] http://www.yourdictionary.com/row?direct_search_result=yes

[8] *Id.*

### J. "trace" ('167 Patent, cl.1, 12; '554 Patent, cl.1‑6)

| Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|
| conductive path on an insulating substrate | conductive line on an insulating substrate |

The parties dispute whether a "trace" is a "path" or a "line." Plaintiff contends "line" might cause the jury to think a "trace" must be straight, and that "path" is consistent with contemporaneous technical and non-technical dictionaries. Pl.'s Br. [Dkt. # 123] at 26–27. Defendants counter that the specification equates "conductive lines" with "traces." Defs.' Br. [Dkt. # 134] at 29–30. Defendants are amenable to clarifying that the "line" in its proposed construction need not be straight. *Id.* at 29 n.5. During the hearing, Plaintiff agreed that clarifying the line need not be straight addressed its major issue with Defendants' construction, although Plaintiff believes "path" would be less confusing for the jury. H'rg Tr. [Dkt. # 178] at 125:1–2.

The Court sees no meaningful distinction between "path" and "line" for this term. But in light of the patent's use of "line" in the specification, and given Plaintiff's agreement that the major claim construction dispute is resolved by recognizing the "line" need not be straight, the Court adopts Defendants' proposed construction of "conductive line on an insulating substrate" and notes the "conductive line" need not be straight.

### K. The "Purpose" Limitations

| Term | Plaintiff's ProposedConstruction | Defendants' Proposed Construction |
|---|---|---|
| to isolate the signal traces and thereby provide noise shielding ('167 Patent, cl.1, 11) | plain meaning, no intent required | for the purpose of providing a shield between the signal traces in order to reduce electrical noise |
| to isolate the signal traces and thereby provide noise shielding ('167 Patent, cl.6, 12) | plain meaning, no intent required | for the purpose of providing a shield between two groups of signals |
| to create a bottom-layer isolating ground trace ('167 Patent, cl.1, 6, 11, 12) | plain meaning, no intent required | for the purpose of creating a bottom-layer isolating ground trace |
| to create a second layer isolating ground trace ('554 Patent, cl.1) | plain meaning, no intent required | for the purpose of creating a second-layer isolating ground trace |
| to provide noise shielding ('554 Patent, cl.1) | plain meaning, no intent required | in order to provide a shield that reduces electrical noise |

The parties dispute whether these phrases require (1) purpose on the part of an accused infringer, or (2) the recited result or effect. Plaintiff argues the "to" clauses describe the result or effect of arranging the components of the claims in the manner recited. Pl.'s Br. [Dkt. # 123] at 28–29. Defendants stress their position—that an accused infringer must have some intent associated with the recited step—has already been adopted in other litigation concerning these patents, and that including the purpose is necessary. Defs.' Br. [Dkt. # 134] at 23.

Plaintiff primarily relies on *Texas Instruments v. I.T.C.*, 988 F.2d 1165 (Fed. Cir. 1993), in which the Federal Circuit considered similarly structured claim language. One claim recited, "whereby the fluid will not directly engage the device and electrical connection means at high velocity, and the conductors will be secured against appreciable displacement by the fluid." *Texas Instruments*, 988 F.2d at 1169. Two of the asserted claims recited injecting a fluid insulating material "to preclude direct high velocity engagement between the fluid and the device and the electrical connections thereto." *Id.* at 1169–70. The court concluded these phrases "merely describe the result of arranging the components of the claims in the manner recited in the claims." *Id.* at 1172; *see also id.* ("A 'whereby' clause that merely states the result of the limitations in the claim adds nothing to the patentability or substance of the claim.").

Defendants rely on two different Federal Circuit opinions to support their position. In *Jansen v. Rexall Sundown, Inc.*, the appellate court construed the preamble as limiting because it gave life and meaning to the claim. 342 F.3d 1329, 1333 (Fed. Cir. 2003). As a result, the court concluded the preamble was not merely a statement of effect, but rather a statement of intentional purpose for which the method must be performed. *Id.* In *Paragon Solutions, LLC v. Timex Corp.*, the appellate court construed "displaying real time data" as "displaying data without intentional delay." 566 F.3d 1075, 1092–93 (Fed. Cir. 2009).

Having considered the parties' briefing and argument on these phrases, the Court finds persuasive Judge Sleet's reasoning in *Invensas Corp. v. Renesas Elecs. Corp.*, No. 11-448-GMS, 2013 WL 3753621 at *2, nn.10–12 (D. Del. July 15, 2013). Accordingly, for

the reasons set forth in Judge Sleet's opinion, the Court adopts Defendants' proposed constructions for these five terms.

## III. ORDER

The Court **ORDERS** each party not to refer, directly or indirectly, to its own or any other party's claim construction positions in the presence of the jury. Likewise, the Court **ORDERS** the parties to refrain from mentioning any part of this opinion, other than the actual positions adopted by the Court, in the presence of the jury. Any reference to claim construction proceedings is limited to informing the jury of the positions adopted by the Court.

**SIGNED this 26th day of October, 2018.**

ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE